Pranav Srinivasan

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EDUCATION

University of Michigan, Ann Arbor

Aug. 2022 – Present

Ph.D. in Computer Science

University of Michigan, Ann Arbor

Sept. 2018 – May 2019

Master of Science in Computer Science

University of Michigan, Ann Arbor

Sept. 2014 - May 2018

Bachelor of Science in Honors Mathematics & Computer Science

EXPERIENCE

Software Engineer, C++ Compiler

Aug. 2019 – Aug. 2022

Microsoft Corporation

Redmond, WA

- Worked on the MSVC C++ Compiler team developing support for x64 Emulation on ARM64
- Helped bring up ARM64EC, a new ABI used to interface with emulated binaries

Graduate Student Research Assistant

Jan. 2019 – May 2019

University of Michigan

Ann Arbor, MI

- Worked on analyzing tradeoffs in size, power, and latency for hardware-level obfuscation security technology
- Assisted in constructing hardware acceleration benchmarks for various military applications

Azure Networking Software Engineering Intern

May 2018 - Aug. 2018

Microsoft Corporation

Redmond, WA

- Worked on autoscaling services running in a virtual cluster based on usage metrics using container technologies (Docker, Kubernetes)
- Built API extensions to a Kubernetes cluster to scale based on metrics output by in-cluster services

System Infrastructure Engineering Intern

May 2017 – Aug. 2017

Bloomberg LP

New York City, NY

• Built a C++ internal use library to allow users to query and update feature-flag bits stored remotely

Research Assistant

May 2016 – Aug. 2016

University of Michigan

Ann Arbor, MI

• Partook in research in combinatorics, specifically dealing with partial ordering properties of permutations that avoid 321 as a substring

Teaching Assistant, EECS 183

Sept. 2015 – Dec. 2018

University of Michigan

Ann Arbor, MI

- Designed and implemented an elevator scheduling course project used by the class for testing C++ proficiency
- Managed website and GitHub infrastructure for student final project submission for a course of 1000+ students
- Conducted weekly office hours and discussion sections for a class of 20-30 students

PROJECTS

Alpha 64 Out-of-Order Processor | System Verilog

Jan. 2018 - May 2018

- Built a SystemVerilog hardware design for a R10K Scheme processor for a subset of the Alpha 64 ISA.
- Expanded design to work on parameterized superscalar and multithread level
- Worked along with 3 other people

EECS 183 Course Infrastructure | Python, Flask, SQLite

Sept. 2016 – Dec 2018

- Built a REST API to manage student team information and validate student's GitHub, submissions, etc.
- Built several scripts to automate assignment tasks formerly done by hand. My favorite such script was a hill-climbing algorithm to fairly distribute grading assignments across staff with different grading skill sets.